IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Rule 53(b) Divisional Application of:

Takashi FUSHIE et al

Serial No.: **(Div. of Serial No.09/579,270 filed May 26, 2000)**

Group Art Unit: **2841(prior)**

Filed: **December 6, 2001**

Examiner: **Patel, I. (prior)**

For: **MULTILAYER PRINTED CIRCUIT BOARD AND THE MANUFACTURING METHOD**

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

December 6, 2001

Sir :

Prior to examination on the merits, please amend the above-identified application as follows:

IN THE CLAIMS

Please CANCEL claims 1-24.

Please ADD claims 25-50 as follows:

25. (New) A process of producing a multilayer printed wiring board, comprising the steps of:

(a) providing a photosensitive glass substrate;

(b) forming through holes by irradiating light onto through-hole portions of the glass substrate through a mask so as to create a latent image corresponding to the exposed portions, and then removing glass of the exposed portions;

(c) crystalizing the glass substrate having the through holes formed, by applying heat-treatment thereto;

(d) forming a plurality of insulating layers and wiring layers on each of opposite surfaces of the crystalized glass substrate; and

(e) coating the through holes with a conductive film to provide conductive connection between the opposite surfaces of the glass substrate.

26. (New) The process according to claim 25, wherein said crystalizing step (c) crystalizes the glass substrate, whereby the coefficient of thermal expansion of the crystalized glass substrate will be close to that of a metallic material constituting the wiring layers.

27. (New) The process according to claim 25, wherein said crystalizing step (c) suppresses ion migration.

28. (New) The process according to claim 25, wherein said layer-forming step (d) forms a plurality of wiring patterns by repeating the substeps of:

(d1) forming a wiring layer on each side of the wiring board in process, creating a resist pattern on the wiring layer, and forming a wiring pattern by using the created resist pattern as a mask; and

(d2) forming an insulating layer on the wiring pattern.

29. (New) The process according to claim 28, wherein the wiring patterns have a line width of 3 μm to 50 μm.

30. (New) The process according to claim 25, further comprising the step of forming a protective layer that covers the conductive film formed in the through holes.

31. The process according to claim 30, wherein protective-layer-forming step uses a screen printing technique.

32. (New) The process according to claim 25, further comprising the step of dealkalizing the glass substrate.

33. (New) The process according to claim 25, wherein said coating step (e) is performed together with said layer-forming step (d), whereby the conductive film and the wiring layer are formed simultaneously.

34. (New) The process according to claim 25, wherein said layer-forming step (d) comprises the substep of forming at least one adhesion-reinforcing layer before forming the wiring layers, so as to provide an enhanced adhesion strength to the wiring layers.

35. (New) The process according to claim 30, further comprising the step of polishing at least one side of the wiring board after the protective layer is formed.

36. (New) The process according to claim 25, further comprising the step of forming a barrier layer on each of the wiring layers for protection thereof.

37. (New)The process according to claim 25, wherein said layer-forming step (d) forms each of the insulating layers on one side of the wiring board at a time.

38. (New) A process of producing a multilayer printed wiring board, comprising the steps of:

(a) providing an alkali-free glass substrate containing no alkali metal ions;

(b) forming through holes on the glass substrate;

(c) forming a plurality of insulating layers and wiring layers on each of opposite surfaces of the crystalized glass substrate; and

(d) coating the through holes with a conductive film to provide conductive connection between the opposite surfaces of the glass substrate.

39. (New) The process according to claim 38, wherein said layer-forming step (c) forms a plurality of wiring patterns by repeating the substeps of:

(c1) forming a wiring layer on each side of the wiring board in process, creating a resist pattern on the wiring layer, and forming a wiring pattern by using the created resist pattern as a mask; and

(c2) forming an insulating layer on the wiring pattern.

40.(New) The process according to claim 39, wherein the wiring patterns have a line width of 3 μm to 50 μm.

41.(New) The process according to claim 38, further comprising the step of forming a protective layer that covers the conductive film formed in the through holes.

42. (New) The process according to claim 38, wherein said coating step (d) is performed together with said layer-forming step (c), whereby the conductive film and the wiring layer are formed simultaneously.

43. (New) The process according to claim 38, wherein said layer-forming step (c) comprises the substep of forming at least one adhesion-reinforcing layer before forming the wiring layers, so as to provide an enhanced adhesion strength to the wiring layers.

44. (New) The process according to claim 41, further comprising the step of polishing at least one side of the wiring board after the protective layer is formed.

45. (New) The process according to claim 38, further comprising the step of forming a barrier layer on each of the wiring layers for protection thereof.

46. (New) The process according to claim 38, wherein said layer-forming step (c) forms each of the insulating layers on one side of the wiring board at a time.

47. (New) A process of producing a multilayer printed wiring board, comprising the steps of:

(a) providing a glass substrate containing alkali metal ions;

(b) forming through holes on the glass substrate;

(c) forming an ion-blocking layer on the glass substrate or dealkalizing the glass substrate to suppress ion migration;

(d) forming a plurality of insulating layers and wiring layers on each of opposite surfaces of the crystalized glass substrate; and

(e) coating the through holes with a conductive film to provide conductive connection between the opposite surfaces of the glass substrate.

48. (New) The process according to claim 47, wherein the ion blocking layer comprises a sputtering silicon nitride layer and a sputtering silicon oxide layer that are formed on the glass substrate in that order.

49. (New) The process according to claim 47, wherein said layer-forming step (d) forms a plurality of wiring patterns by repeating the substeps of:

(d1) forming a wiring layer on each side of the wiring board in process, creating a resist pattern on the wiring layer, and forming a wiring pattern by using the created resist pattern as a mask; and

(d2) forming an insulating layer on the wiring pattern.

50. (New) The process according to claim 47, further comprising the step of forming a protective layer that covers the conductive film formed in the through holes.

REMARKS

Please enter this amendment before consideration of the merits. Allowance of the claims, at an early date, is requested. In the event this paper is not timely filed, then this paper is a petition for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper may be charged to Deposit Account No. 01-2340. Favorable consideration and allowance are respectfully solicited.

Respectfully submitted,

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